

REMARKS

Claims 1-21 are pending. Applicants respectfully submit claims 1-21 are patentable over Chan (U.S. 6,057,212) in view of Talwar (U.S. 6,300,208) under 35 U.S.C. 103(a). More specifically, Chan and Talwar fail to teach or suggest all features of all independent claims 1, 13, 16, and 21.

With respect to claims 1-12 and 21, Chan and Talwar fail to teach or suggest making first and second current electrodes electrically active by receiving heat from an energy absorbing layer, as stated in independent claims 1 and 21. The Examiner contends that Chan's absorbing layer is either element 5 or 320. Assuming the Examiner is correct in this assertion, Chan's energy absorbing layers 5 and 320 do not electrically activate any current electrodes. Elements 5 and 320 are a back-plate used as a top surface of one wafer to bond with a back gate-oxide on another wafer. (Column 4, lines 10-14, lines 36-45; Column 5, lines 23-26). Talwar fails to teach or suggest an energy absorbing layer and is relied upon because Talwar teaches annealing a substrate to activate source/drain regions. Talwar, however, fails to use an energy absorbing layer and simply uses the heat from the anneal process instead. Furthermore, there is no motivation to use the energy absorbing layers 5 and 320 from Chan in Talwar's process because neither reference teaches or suggests using an energy absorbing layer to activate source/drain regions. Such a suggestion is found in Applicants' specification and using Applicant's specification to combine discrete elements of the prior art without any teaching or suggestion from the prior art is improper hindsight analysis. Thus, Chan and Talwar, alone or together, fail to teach or suggest using an energy absorbing layer to activate any current electrodes, such as source or drain regions. Claims 1-12 and 21, therefore, are patentable over Chan and Talwar under 35 U.S.C. 103(a).

With respect to claim 21, Chan and Talwar fail to teach or suggest at least another feature. More specifically, Chan and Talwar fail to teach or suggest reducing the resistivity less than 0.001 Ohm-centimeters. Thus, claim 21 is patentable for yet another reason over Chan and Talwar under 35 U.S.C. 103(a).

With respect to claims 13-15, Chan and Talwar fail to teach or suggest all features of independent claim 13. More specifically, Chan and Talwar fail to teach or suggest heating first and second current electrodes using an energy absorbing layer as stated in independent claim 13. As discussed above, Chan and Talwar fail to teach or suggest using an energy absorbing layer to

heat current electrodes. At best, the combination teaches using a metal layer to absorb energy to form a bonded wafer and later forming source and drain region in the bonded wafer, where the source and drain regions are annealed. Thus, claims 13-15 are patentable over Chan and Talwar under 35 U.S.C. 103(a).

With respect to claims 16-20, Chan and Talwar fail to teach or suggest all features of independent claim 16. More specifically, Chan and Talwar fail to teach or suggest a making a semiconductor electrode active from heat provided by an energy absorbing layer. As discussed above, Chan and Talwar fail to teach or suggest providing heat from an energy absorbing layer to any other element or structure. Thus, claims 16-20 are patentable over Chan and Talwar under 35 U.S.C. 103(a).

Believing to have responded to every issue raised by the Examiner, Applicants believe the present Application is currently in a condition of allowance and earnestly solicit allowance of claims 1-21. Please contact Applicant's practitioner listed below if there are any issues.

Respectfully submitted,

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**ALL ITEMS MARKED WITH AN "X" ARE INCLUDED:**

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EXAMINER: Jose R. Diaz  
GROUP ART UNIT: 2815  
SERIAL NO.: 10/085,889  
FILED: FEBRUARY 28, 2002  
INVENTOR: MICHAEL J. RENDON